

## Claims

- [c1] 1. A superjunction Schottky device, comprising:
  - a back metal layer;
  - a semiconductor substrate of a first conductivity type on the back metal layer;
  - a plurality of superjunction cells on the semiconductor substrate, including a plurality of charge-balance layers that extend substantially vertically;
  - a lightly-doped junction barrier Schottky (JBS) region of the first conductivity type on each superjunction cell;
  - and
  - a front conductor layer over the substrate, contacting with the JBS region to form a Schottky contact with the JBS region.
- [c2] 2. The superjunction Schottky device of claim 1, further comprising a plurality of isolation structures, wherein each isolation structure is between two superjunction cells and between two JBS regions.
- [c3] 3. The superjunction Schottky device of claim 2, wherein each isolation structure comprises a material selected from the group consisting of doped and undoped oxide, nitride and polysilicon, and combinations thereof.

- [c4] 4. The superjunction Schottky device of claim 2, wherein each superjunction cell comprises a first layer of a second conductivity type, a second layer of the first conductivity type, a lightly-doped third layer of the first conductivity, a fourth layer of the first conductivity type and a fifth layer of the second conductivity type arranged in sequence.
- [c5] 5. The superjunction Schottky device of claim 4, further comprising a guard ring of the second conductivity type at periphery of each Schottky contact above a superjunction cell.
- [c6] 6. The superjunction Schottky device of claim 5, wherein the JBS region is contiguous with the third layer of the superjunction cell, and the guard ring is over the first, second, fourth and fifth layers of the superjunction cell.
- [c7] 7. The superjunction Schottky device of claim 2, wherein each superjunction cell comprises a first layer of a second conductivity type, a second layer of the first conductivity type and a third layer of the second conductivity type arranged in sequence.
- [c8] 8. The superjunction Schottky device of claim 7, wherein the JBS region is located on the second layer of the superjunction cell, and the first and third layers of the su-

perjunction cell extend upward to periphery of the JBS region.

- [c9] 9. The superjunction Schottky device of claim 8, further comprising a guard ring of the second conductivity type at periphery of each Schottky contact above a superjunction cell.
- [c10] 10. The superjunction Schottky device of claim 1, wherein the superjunction cells are arranged adjacent to each other.
- [c11] 11. The superjunction Schottky device of claim 10, wherein each superjunction cell comprises a first layer of a second conductivity type, a second layer of the first conductivity type, a lightly-doped third layer of the first conductivity, a fourth layer of the first conductivity type and a fifth layer of the second conductivity type arranged in sequence.
- [c12] 12. The superjunction Schottky device of claim 11, further comprising a guard ring of the second conductivity type at periphery of each Schottky contact above a superjunction cell.
- [c13] 13. The superjunction Schottky device of claim 12, wherein the JBS region is contiguous with the third layer of the superjunction cell, and the guard ring is over the

first, second, fourth and fifth layers of the superjunction cell.

- [c14] 14. The superjunction Schottky device of claim 10, wherein each superjunction cell comprises a first layer of a second conductivity type, a second layer of the first conductivity type, a third layer of the second conductivity type arranged in sequence.
- [c15] 15. The superjunction Schottky device of claim 14, further comprising a guard ring of the second conductivity type at periphery of each Schottky contact above a superjunction cell.
- [c16] 16. The superjunction Schottky device of claim 15, wherein the JBS region is located on the second layer of the superjunction cell, and the guard ring is over the first and third layers and a portion of the second layer of the superjunction cell.
- [c17] 17. The superjunction Schottky device of claim 14, wherein the JBS region comprises a lightly doped region of the first conductivity type over all superjunction cells.
- [c18] 18. The superjunction Schottky device of claim 1, wherein a doping concentration in the superjunction cells ranges from  $1\times 10^{15}/\text{cm}^3$  to  $1\times 10^{17}/\text{cm}^3$ .

- [c19] 19. The superjunction Schottky device of claim 1, further comprising an edge termination of the first conductivity type on a peripheral portion of the substrate.
- [c20] 20. The superjunction Schottky device of claim 1, wherein the superjunction cells are located in an epitaxial silicon layer.
- [c21] 21. The superjunction Schottky device of claim 1, wherein the front conductor layer comprises a metal layer forming the Schottky contact with the JBS region.
- [c22] 22. The superjunction Schottky device of claim 1, wherein the front conductor layer comprises a metal silicide layer forming the Schottky contact with the JBS region and a metal layer on the metal silicide layer.
- [c23] 23. The superjunction Schottky device of claim 22, wherein the metal silicide layer contains a metal selected from the group consisting of Au, Pt, Ni, Ti, W, Co, Rh, Pd, Zr, Ta, Cr, Mo and alloys of the above metals with various weight ratios.
- [c24] 24. The superjunction Schottky device of claims 22, wherein the metal layer comprises Al, Al/Si alloy, Al/Si/Cu alloy, Mo/Al alloy, Al/Ni/Au alloy, or Ti/Ni/Ag alloy.

[c25] 25. A method for fabricating a superjunction Schottky device, comprising:

providing a semiconductor substrate of a first conductivity type;

forming a plurality of superjunction cells on a front side of the substrate, the superjunction cells including a plurality of charge-balanced layers that extend substantially vertically;

forming a lightly-doped junction barrier Schottky (JBS) region of the first conductivity type on each superjunction cell;

forming a front conductor layer over the substrate, the front conductor layer contacting with the JBS region to form a Schottky contact with the JBS region; and

forming a back metal layer on a back side of the substrate.

[c26] 26. The method of claim 25, wherein the step of forming the superjunction cells comprises:

forming a lightly-doped semiconductor layer of the first conductivity type on the substrate;

forming a plurality of trenches in the semiconductor layer to define a plurality of active regions;

forming first layers of the first conductivity type in side-walls of each active region;

forming a second layer of a second conductivity type in

an outward sidewall of each first layer; and  
filling each trench with a refill material to form an isolation structure.

- [c27] 27. The method of claim 26, wherein the semiconductor layer between the first layers in each active region directly serves as a JBS region.
- [c28] 28. The method of claim 27, further comprising forming a guard ring of the second conductivity type at periphery of each JBS region over the first and second layers.
- [c29] 29. The method of claim 26, wherein the first layers of the first conductivity type in sidewalls of each active region are merged together to form a third layer of the first conductivity type.
- [c30] 30. The method of claim 29, wherein in each active region, the JBS region is formed in a top portion of the third layer between the second layers by performing an ion implantation of the second conductivity type.
- [c31] 31. The method of claim 30, further comprising forming a guard ring of the second conductivity type at periphery of the JBS region over the second layers.
- [c32] 32. The method of claim 26, wherein the refill material is selected from the group consisting of doped and un-

doped oxide, nitride and polysilicon, and combinations thereof.

- [c33] 33. The method of claim 25, wherein the step of forming the superjunction cells comprises:
  - (a) forming a lightly-doped semiconductor sub-layer of the first conductivity type over the substrate;
  - (b) forming a plurality of first layers of the first conductivity type and a plurality of second layers of a second conductivity type that extend substantially vertically in the semiconductor sub-layer, wherein one second layer is formed between two first layers; and repeating steps (a) and (b) with the first and second layers in each semiconductor sub-layer being aligned to increase a height of the first and second layers, until a predetermined height is obtained.
- [c34] 34. The method of claim 33, wherein one first layer is formed between one second layer and an unimplanted portion of the semiconductor layer, and the unimplanted portion directly serves as a JBS region.
- [c35] 35. The method of claim 34, further comprising forming a guard ring of the second conductivity type at periphery of each JBS region over the first and second layers.
- [c36] 36. The method of claim 33, wherein the first layers and

the second layers are arranged alternately, and each JBS region is formed in a top portion of a first layer between two second layers.

- [c37] 37. The method of claim 36, further comprising forming a guard ring of the second conductivity type at periphery of the JBS region over the second layers.
- [c38] 38. The method of claim 33, wherein forming the Schottky shift region comprises:
  - forming a lightly-doped semiconductor layer of the first conductivity type on all superjunction cells as a JBS region.
- [c39] 39. The method of claim 25, wherein forming the front conductor layer comprises:
  - forming a blocking layer over the substrate exposing the JBS region; and
  - forming a metal layer contacting with the Schottky shift region using the blocking layer as a mask.
- [c40] 40. The method of claim 25, wherein forming the front conductor layer comprises:
  - forming a blocking layer over the substrate exposing the JBS region;
  - forming a metal silicide layer contacting with the JBS region using the blocking layer as a mask; and

forming a metal layer on the metal silicide layer.

- [c41] 41. The method of claim 40, wherein the metal silicide layer contains a metal selected from the group consisting of Au, Pt, Ni, Ti, W, Co, Rh, Pd, Zr, Ta, Cr, Mo and alloys of the above metals with various weight ratios.
- [c42] 42. The method of claims 40, wherein the metal layer comprises Al, Al/Si alloy, Al/Si/Cu alloy, Al/Ni/Au alloy, Cr/Ni/Ag alloy or Ti/Ni/Ag alloy.
- [c43] 43. The method of claim 25, wherein a doping concentration in the superjunction cells ranges from  $1\times10^{15}/\text{cm}^3$  to  $1\times10^{17}/\text{cm}^3$ .
- [c44] 44. The method of claim 25, further comprising forming an edge termination on a peripheral portion of the substrate.
- [c45] 45. The method of claim 25, wherein the superjunction cells and the JBS region are formed in an epitaxial silicon layer.